

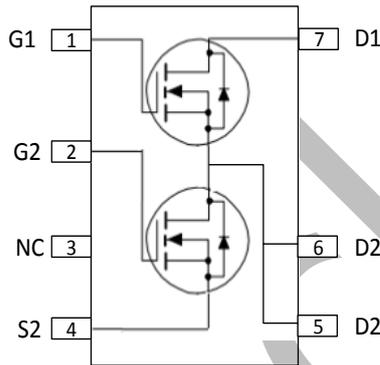
## Features

- Output MOSFET voltage: 600V
- Driver output current (DC) : 2A
- $R_{ds(on)}=4.5 \Omega$  @  $V_{GS}=10V$
- High staturation current
- Operating ambient temperature  
-  $T_A=-40^{\circ}C$  to  $105^{\circ}C$  (G: Industrial application)
- Dual N-channel mos
- package: DIP7/SOP6

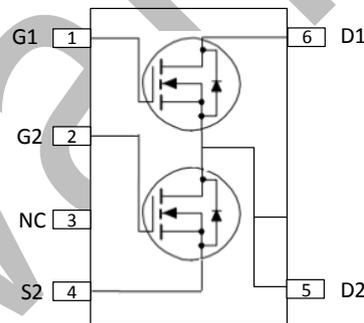
# 1 Introduction

These dual N-Channel enhancement mode power field effect transistors are particularly suited for high voltage applications for motor driving. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast swithing.

The blockdiagram as follows:



**Featur 1 DIP7 package**



**Featur 2 SOP6 package**

The absolute maximum rating as follow table shows:

**Absolute Maximum Ratings** (T<sub>j</sub>= 25°C, unless otherwise specified)

Parameter	Symbol	Rating	Units
Drain-to-Source Voltage	V <sub>DSX</sub>	600	V
Continuous Drain Current T <sub>C</sub> = 25 °C	I <sub>D</sub>	2	A
Continuous Drain Current T <sub>C</sub> = 100 °C	I <sub>D</sub>	1.2	A
Pulsed Drain Current	I <sub>DM</sub> <sup>a1</sup>	8	A
Gate-to-Source Voltage	V <sub>GS</sub>	±30	V
Power Dissipation(T <sub>c</sub> =25°C)	P <sub>tot</sub>	35	W
Operating Junction	T <sub>j</sub>	150	°C
Junction to Ambient	J <sub>a</sub>	74.29	°C/W
Single Pulse Avalanche Energy	E <sub>as</sub>	90	mJ

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## 2 Electrical Characteristics

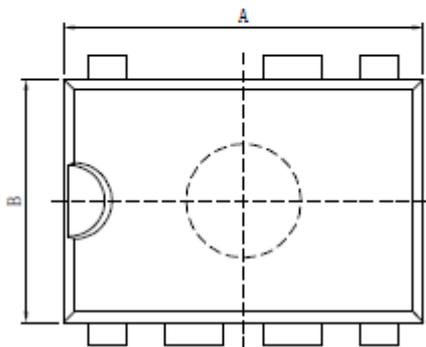
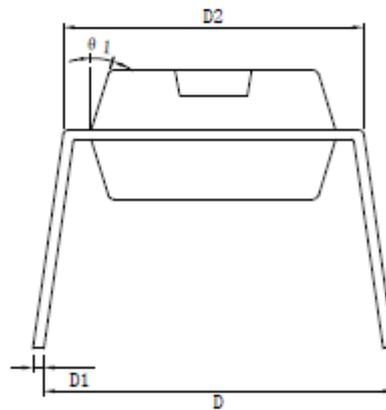
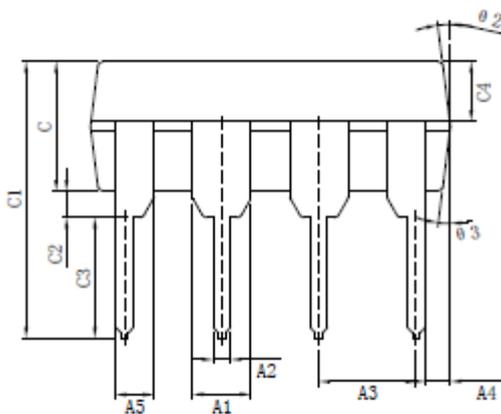
Parameter	Symbol	Test Conditions	Rating			Units
			Min	Typ	Max	
Drain-to-Source Breakdown Voltage	$V_{DS}$	$V_{GS}=0V, I_D=250\mu A$	600			V
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=1.0A$		4.5	5.0	$\Omega$
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	3.5	4.0	4.5	V
Drain-to-Source Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_{DS}=2A$			1.5	V
Drain to Source Leakage Current	$I_{DSS}$	$V_{DS}=600V, V_{GS}=0V, T_c=25^\circ C$			1	$\mu A$
		$V_{DS}=480V, V_{GS}=0V, T_c=125^\circ C$			100	$\mu A$
Gate to Source Forward Leakage	$I_{GSS(F)}$	$V_{GS}=+30V$			100	nA
Gate to Source Reverse Leakage	$I_{GSS(R)}$	$V_{GS}=-30V$			-100	nA
Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$		438		pF
Output Capacitance	$C_{oss}$			34		pF
Reverse Transfer Capacitance	$C_{riss}$			1.3		pF
a: Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						
Parameter	Symbol	Test Conditions	Rating			Units
			Min	Typ	Max	
Reverse Recovery Time	$T_{rr}$	$di/dt = 100A/\mu s, I_S = 2A$		45	100	ns
Reverse Recovery Charge	$Q_{rr}$			50		nC
Reverse Recovery Current	$I_{RRM}$			2.3		A
a: Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						

### 3 Package information

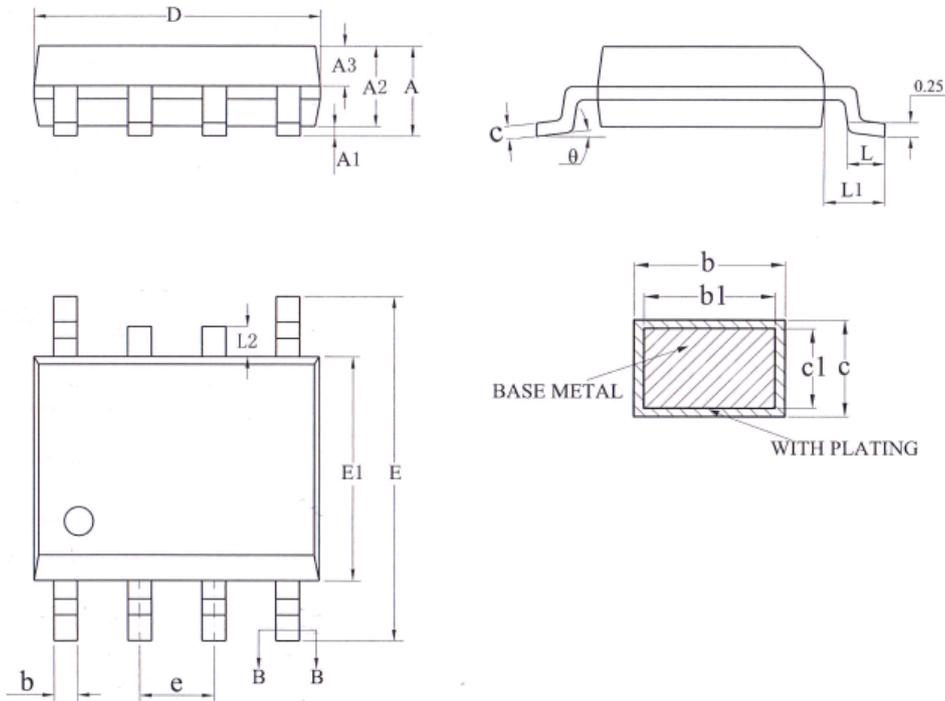
ACP9122 provide DIP7 package.

#### 3.1 DIP7 package information

type \ size	min(mm)	max(mm)		min(mm)	max(mm)
A	9.00	9.20	C2	0.50TYP	
A1	1.474	1.574	C3	3.20	3.40
A2	0.41	0.51	C4	1.47	1.57
A3	2.44	2.64	D	8.20	8.80
A4	0.51TYP		D1	0.244	0.264
A5	0.99TYP		D2	7.62	7.87
B	6.10	6.30	θ 1	17° TYP4	
C	3.20	3.40	θ 2	10° TYP4	
C1	7.10	7.30	θ 3	8° TYP	



### 3.2 SOP6 package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.50	—	0.80
L1	1.05REF		
L2	0.30	0.40	0.50
$\theta$	0	—	8°

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## 4 Revision history

version	Name	Date	Changes
V1.0	Daniel	2023-3-1	initial version

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